# Midterm Exam

(February 15th @ 7:30 pm)

Presentation and clarity are very important! Show your procedure!

## PROBLEM 1 (19 PTS)

- Compute the result of the following operations. The operands are signed fixed-point numbers. The result must be a signed fixed-point number. For the division, use $x = 5$ fractional bits.

| | | |
|---|---|---|
| 1.0111 + 1.101010 | 1.010110 − 1000.0101 | 01.11111 + 0.10011 |
| 1.01101 × 10.101 | 0.111 × 1.0101 | 01.011 ÷ 1.011 |

## PROBLEM 2 (11 PTS)

- Represent these numbers in Fixed Point Arithmetic (signed numbers). Use the FX format [8 4]. Truncate (the LSB) and perform Saturation when required.
  - ✓ -33.375
  - ✓ 17.875

- Complete the table for the following fixed-point formats (signed numbers): (3 pts.)

| Integer bits | Fractional Bits | FX Format | Range | Resolution |
|---|---|---|---|---|
| 6 | 4 | | | |

- Given the 32-bit floating-point number: **ECE4710A**. Complete the bits in the fields and the significand's FX format: (3 pts.)

sign e+bias

FX format of significand: _____

significand

## PROBLEM 3 (40 PTS)

- Perform the following 32-bit floating point operations. For fixed-point division, use 4 fractional bits. Truncate the result when required. Show your work: how you got the significand and the biased exponents bits of the result. Provide the 32-bit result.

| | | | |
|---|---|---|---|
| ✓ 4F480000 + D0A90000 | ✓ C1500000 − C36A0000 | ✓ FABC0000 × 80400000 | ✓ 7BB80000 ÷ C9400000 |

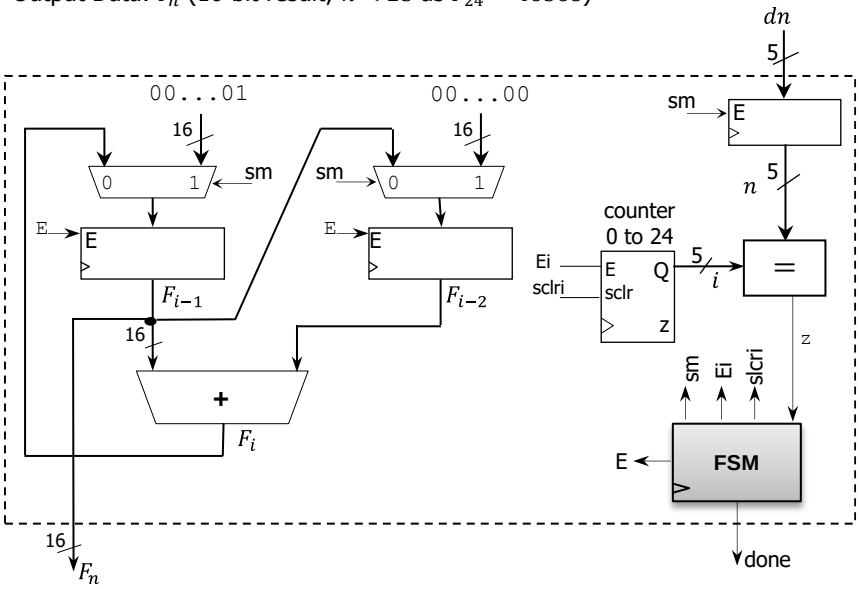
## PROBLEM 4 (30 PTS)

- **Fibonacci numbers Computation**: This circuit reads an unsigned number ($n > 1$) and generates $F_n$:

$$F_n = F_{n-1} + F_{n-2},\ F_0 = 0,\ F_1 = 1$$

- The digital system is depicted below (FSM + Datapath).
  - ✓ Input Data $dn$ ($1 < dn < 25$). Output Data: $F_n$ (16-bit result; $n < 25$ as $F_{24} = 46368$)
  - ✓ $z = 1$ when $i = n$.
  - ✓ Sequential Algorithm:

```
n: unsigned integer
F0=0, F1=1
if n > 1
    for i = 2 to n
        Fi = Fi-1 + Fi-2
    end
end
return Fn
```



- Sketch the Finite State Machine diagram (in ASM form) given the sequential algorithm. (15 pts.)
  - ✓ The process begins when the $\mathrm{s}$ signal is asserted, at this moment we capture $dn$ on register $n$. At the same time, the registers $F_{i-1}$ and $F_{i-2}$ are initialized with $1$ and $0$ respectively. Then, the process continues by updating $F_{i-1}$ and $F_{i-2}$, and it is concluded when $i = n$. The signal $\mathrm{done}$ is asserted when the result is ready and appears on output $F_n$.
    - Note that the iteration index $i$ index must start at $i = 2$.

- Complete the timing diagram. $n$ is provided as an unsigned decimal. You can provide $F_{i-1}$, $F_{i-2}$, and $i$ as unsigned decimals. (15 pts.)